An Improvement of IM and Power of High Power Amplifiers Using RC-Paralleled Circuits with Frequency Selectivity

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Abstract

This paper describes the design method to improve IM and power of high power amplifiers by employing a RC-paralleled circuit with frequency selectivity in the design of input matching circuits. The RC-paralleled circuit decreases gain at low frequencies where the power level of inter-modulated signals becomes high, leading to a significant improvement of IM and power.

Introduction

In the design of high power amplifiers for use in mobile and satellite communication systems, high linearity is required to reduce adjacent channel interference. The conventional linear power amplifier design have focused on improving linearity around carrier frequencies by using predistortion or feed-forward linearizers [1-2]. Recently some works have stated the importance to design matching circuits including bias circuits at low frequencies where the power level of inter-modulated signals becomes high [4,5]. These works, however, have addressed only the output matching conditions though the low frequency inter-modulated signals appear in both input and output matching circuits. In the case when high power amplifiers have a high gain at these low frequencies, the low frequency inter-modulated signals of the input matching circuit are amplified and provide a serious effect on IM and power.

To address this problem, a RC-paralleled circuit with frequency selectivity is employed in series with FETs' gate for decreasing gain at low frequencies where the power level of inter-modulated signals becomes high. In addition, a series resistor is employed in the design of gate bias circuits for the same reason. With the use of the RC-paralleled circuit and a series resistor, an improvement of IM_3 up to 4.7 dB and output power up to 1 dB has been achieved for the C-band 10W GaAs FET amplifier.

Low Frequency Components of Inter-Modulated Singals

It is well known that the inter-modulated signals are nf_1+mf_2 in two-tone excitation ($f_1 < f_2$, n and m are integer). Among these inter-modulated signals, the low frequency components are n times of separation frequency, that is, f_2-f_1, $2(f_2-f_1)$, $3(f_2-f_1)$, --- . The frequency separation of two tones is f_2-f_1, which is expressed as Δf. In the case when terminations of high power amplifier becomes short at low frequency, the voltage of the low frequency inter-modulated signals becomes zero, not degrading IM and power characteristics. In the actual case, however, it becomes difficult to make the impedances of matcihg circuits ideally short at these low frequencies. Therefore, the low frequency inter-modulated signals vary the gate and drain bias conditions and degrade IM and power performance.

As an example, time-domain waveforms of the gate and drain voltages of the 7-GHz 10 W GaAs FET amplifier were measured below 1 GHz at nodes g_1,d_1, respectivly and is shown in Fig. 1, where Δf is 150 MHz and the impedance of the input and output matching circuits is not ideally short below 1 GHz. The variation of the gate voltage is -2.5+/-0.4 V and that of the drain voltage is 9+/-3.7 V. It is clearly shown that the lowest inter-modulated signal (Δf) appears in both input and output matching circuits, which is considered to have a serious effect on IM and power performance

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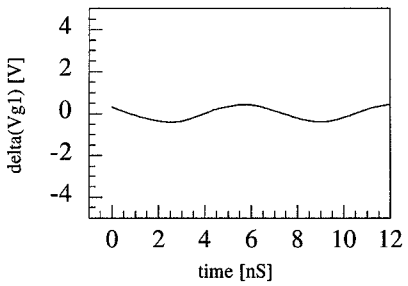
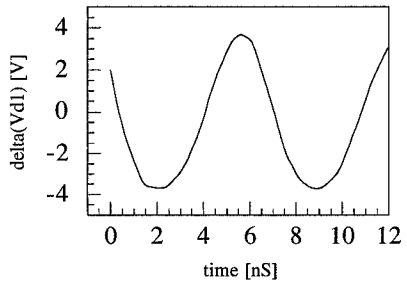


(a) Wave form of gate (g_1)



(b) Wave form of drain (d_1)

Fig. 1 Time-domain waveforms of the gate and drain voltages of the 7-GHz 10W GaAs FET amplifier.

Design of RC-Paralleled Circuits

A schematic diagram of the 7-GHz 10W GaAs FET amplifier with a RC-paralleled circuit is shown in Fig. 2. The amplifier is comprised of four of the 18.9 mm GaAs MESFETs, input and output matching circuits, gate and drain bias circuits, and a RC-paralleled circuit. To improve IM and power of the amplifier, the impedance of input and output matching circuits has to be short at Δf, 2Δf, 3Δf, ---. That is, the values of the bypass capacitors (C_g and C_d) have to be designed as large as possible. Then the value of the series resistor (R_g) of the gate bias circuit is designed to minimize gain at Δf, 2Δf, 3Δf, ---. Finally, a RC-paralleled circuit is connected in series with FETs' gate to selectively decrease gain at Δf, 2Δf, 3Δf, ---. The condition that the RC-paralleled circuit becomes resistive at a low frequency (f_L) and capacitive at a high frequency (f_H) is as follows:

$$\frac{1}{2\pi f_H}\left(=K_H\right) < K < \frac{1}{2\pi f_L}\left(=K_L\right) \qquad (1)$$

where K = RC. In the case of the 7-GHz 10 W GaAs FET amplifier with Δf = 150 MHz, f_L is 150 MHz and f_H is 7

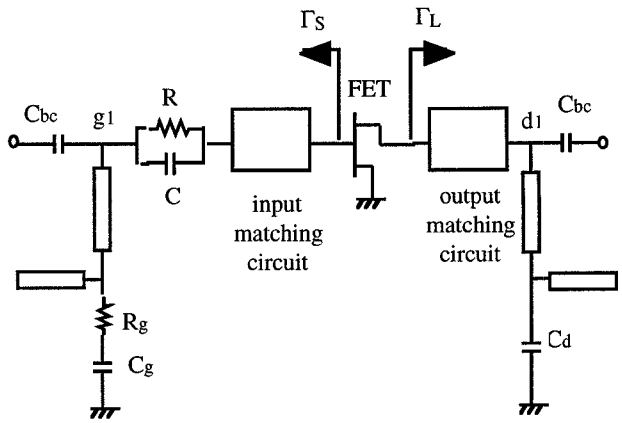


Fig. 2 Schematic diagram of the 7-GHz 10W GaAs FET amplifier with a RC-paralleled Circuit.

GHz. The range of K satisfying the condition (1) with a parameter of R and C is shown in Fig. 3. In addition, the insertion loss of the RC-paralleled circuit is calculated for a constant value of K and is shown in Fig. 4. It is noted in Fig. 4 that a low value of C and a high value of R are desirable to maximize the insertion loss at f_L and minimize the insertion loss at f_H However, a high value of R causes a gate bias variation due to a gate current (I_{gs}) under large-signal operation. Therefore, the values of R and C were obtained to keep |(R+Rg)Igs| < 0.1 V in addition to maximizing the insertion loss at f_L and minimizing the insertion loss at f_H within the range of K shown in Fig. 2. The final values of R and C were R = 50Ω and C = 9.1 pF. The gain

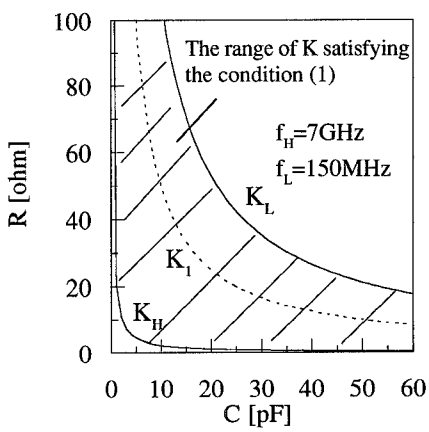


Fig. 3 Range of K satisfying the condition (1) with a parameter of R and C.

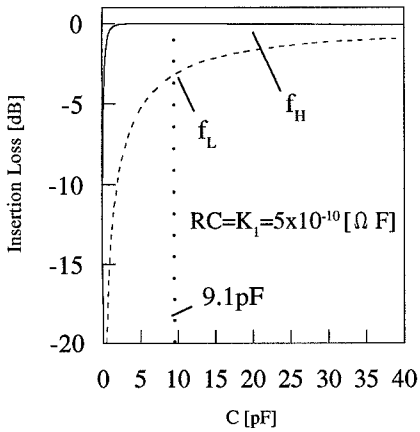


Fig. 4 Insertion loss of the RC-paralleled circuit.

of the 7-GHz 10W GaAs FET amplifier with and without using the RC-paralleled circuit are calculated for the schematic diagram shown in Fig. 1. The calculated results are shown in Fig. 5. The small-signal model parameters of the 18.9 mm GaAs MESFET are summarized in Table 1. The values of C_g and C_d were determined to 0.1μ F. The value of R_g was determined to 5Ω. The measured results are also shown in Fig. 5. It is clearly shown that the gain can be reduced to 20 dB for Δf = 120 to 150 MHz with the use of the RC-paralleled circuit.

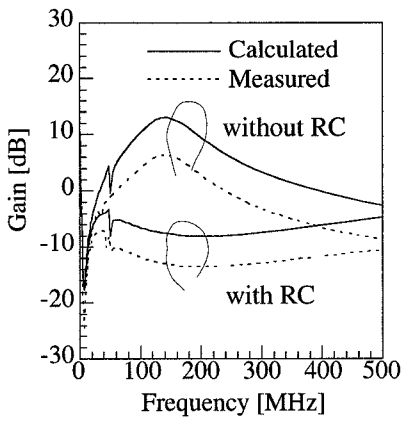


Fig. 5 Gain of the 7-GHz 10W GaAs FET amplifier at low frequency with and without using the RC-paralleled circuit.
RC-paralleled circuit : R=50Ω,C=9.1pF
Cg=Cd=0.1μF ,Rg=5 Ω

Table 1Small-signal model parameters of the 18.9 mm GaAs MESFET.

Wg		18.9mm
Lg	(nH)	0.016
Ld	(nH)	0.026
Ls	(nH)	0.001
Cgs	(pF)	16.8
Cdg	(pF)	0.78
Cds	(pF)	3.1
Cgsd	(pF)	0.025
Cdsd	(pF)	0.015
Rg	(ohm)	0.3
Ri	(ohm)	0.31
Rs	(ohm)	0.02
Rd	(ohm)	0.4
Rds	(ohm)	10.4

Improvement of IM and Power

The measured output power (P_{out}) and variations of the gate and drain voltages (V_g and V_d) of the 7-GHz 10W GaAs FET amplifier with and without using the RC-paralleled circuit are shown in Fig. 6, where Δf is varied from 0 to 150 MHz. The output power was improved up to 0.6 dB by using the RC-paralleled circuit for an input power of 35 dBm. The variation of V_d (ΔV_{dl}) were also improved up to 2.0V. For Δf = 120 to 130 MHz, the output power was greatly improved, which corresponds to the gain reduction

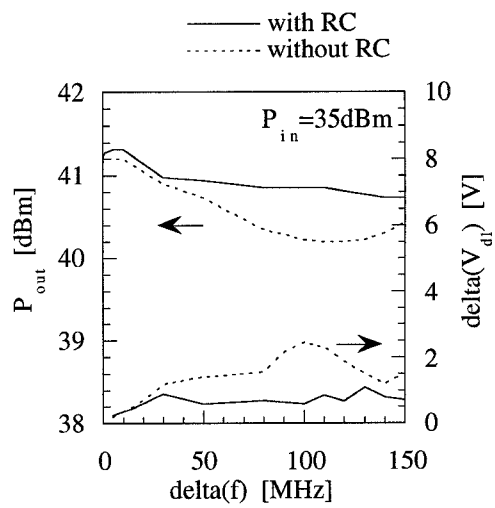


Fig. 6 Output power and variations of the gate and drain voltages of the 7-GHz 10W GaAs FET amplifier with and without using the RC-paralleled circuit.

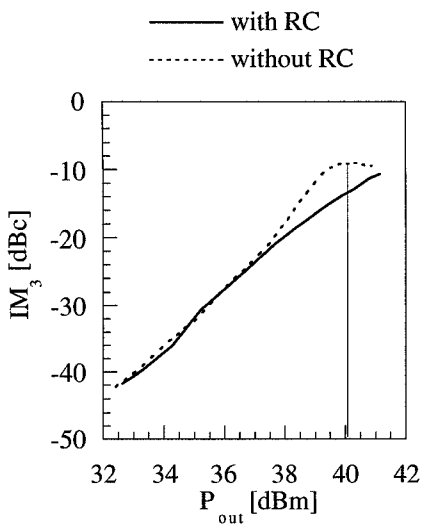


Fig. 7 Measured IM_3 vs P_{out} at $\Delta f = 120$ MHz.

shown in Fig. 5. The measured IM_3 vs P_{out} at $\Delta f = 120$ MHz is plotted in Fig. 7. The improvement of IM_3 with the RC-paralleled circuit was 4.7 dB at $P_{out} = 40$ dBm.

Conclusioin

We have presented the design method to improve IM and power of high power amplifiers by employing the RC-paralleled circuit with frequency selectivity in the design of input matching circuits. It has been clearly shown in experiment that the RC-paralleled circuit selectively decreases gain at low frequencies where the power level of inter-modulated signals becomes high and improves the variation of the gate and drain voltages, leading to the significant improvement of IM and power performance.

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